



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.:	8333
Jensen <i>et al.</i>	Art Unit:	2183
Appl. No.: 09/702,112	Examiner:	Ellis, Richard L.
Filed: October 30, 2000	Atty. Docket:	1778.1730000
For: Boundary Address Registers for Selection of ISA Mode		

Supplemental Information Disclosure Statement

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application

does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b) before the mailing of a first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114. No statement or fee is required.

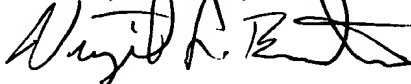
Copies of documents AK1-AR1, AK2, AN2-AR2, and AN3 are provided. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the accompanying Form PTO-1449 are provided.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



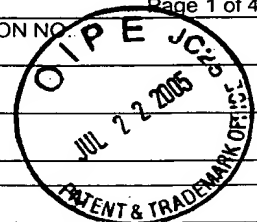
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Date: 7/22/05

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FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1778.1730000	APPLICATION NO. 09/702,112
	FIRST NAMED INVENTOR Michael Gottlieb Jensen	ART UNIT 2183
	FILING DATE October 30, 2000	



U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	3,794,980	02/1974	Cogar <i>et al.</i>			
	AB1	3,811,114	05/1974	Lemay <i>et al.</i>			
	AC1	3,840,861	10/1974	Amdahl <i>et al.</i>			
	AD1	3,983,541	09/1976	Faber <i>et al.</i>			
	AE1	4,110,822	08/1978	Porter <i>et al.</i>			
	AF1	4,149,244	04/1979	Anderson <i>et al.</i>			
	AG1	4,229,790	10/1980	Gilliland <i>et al.</i>			
	AH1	4,295,193	10/1981	Pomerene, James H.			
	AI1	4,432,056	02/1984	Aimura, Harutsugu			
	AJ1	4,467,409	08/1984	Potash <i>et al.</i>			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK1	EP 0 073 424 A2	03/1983	Europe			N/A
	AL1	EP 0 239 081 B1	09/1995	Europe			N/A
	AM1	EP 0 368 332 B1	09/1997	Europe			N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN1	U.S. Utility Patent Application No. 09/702,115, inventors Jensen, M., <i>et al.</i> , filed October 30, 2000 (not published) (71 pages).
	AO1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).
	AP1	Preliminary Amendment, filed February 1, 2002, in U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (15 pages).
	AQ1	Case, Brian, "ARM Architecture Offers High Code Density: Non-traditional RISC Encodes Many Options in Each Instruction," <i>Microprocessor Report</i> , Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).
	AR1	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor Forum, 13 slides (7 pages) (October 22-23, 1996).

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	4,507,728	03/1985	Sakamoto <i>et al.</i>			
	AB2	4,685,080	08/1987	Rhodes, Jr. <i>et al.</i>			
	AC2	4,724,517	02/1988	May, Michael D.			
	AD2	4,777,594	10/1988	Jones <i>et al.</i>			
	AE2	4,782,441	11/1988	Inagami <i>et al.</i>			
	AF2	5,132,898	07/1992	Sakamura <i>et al.</i>			
	AG2	5,241,636	08/1993	Kohn, Leslie D.			
	AH2	5,355,460	10/1994	Eickemeyer <i>et al.</i>			
	AI2	5,463,700	10/1995	Nakazawa, Tamotsu			
	AJ2	5,467,134	11/1995	Laney <i>et al.</i>			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK2	EP 0 449 661 B1	11/1995	Europe			N/A
	AL2						Yes No
	AM2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).
	AO2	Kurosawa, K., <i>et al.</i> , "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," <i>Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988)</i> , MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).
	AP2	LSI TinyRisc Development (visited April 24, 2001), at http://www.redhat.com/support/manuals/gnupro99rl/6_embed/emb09.html , 13 pages.
	AQ2	NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright NEC Electronics Corporation 2000) (76 pages).
	AR2	NEC User's Manual, VR4100 Series TM , 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 (Chapter 3) (Copyright NEC Corporation 2002).

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	5,506,974	04/1996	Church <i>et al.</i>			
	AB3	5,546,552	08/1996	Coon <i>et al.</i>			
	AC3	5,574,873	11/1996	Davidian, Gary G.			
	AD3	5,577,200	11/1996	Abramson <i>et al.</i>			
	AE3	5,619,666	04/1997	Coon <i>et al.</i>			
	AF3	5,732,234	03/1998	Vassiliadis <i>et al.</i>			
	AG3	5,751,932	05/1998	Horst <i>et al.</i>			
	AH3	5,794,010	08/1998	Worrell <i>et al.</i>			
	AI3	5,896,519	04/1999	Worrell, Frank			
	AJ3	5,948,112	09/1999	Shimada <i>et al.</i>			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK3						Yes No
	AL3						Yes No
	AM3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN3	Ross, Roger, "There's no risk in the future for RISC," <i>Computer Design</i> , Vol. 28, No. 22, pp. 73-75 (November 13, 1989).
	AO3	
	AP3	
	AQ3	
	AR3	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	5,982,459	11/1999	Fandrianto <i>et al.</i>			
	AB4	6,266,765 B1	07/2001	Horst, Robert W.			07/07/2000
	AC4	6,272,620 B1	08/2001	Kawasaki <i>et al.</i>			04/04/2000
	AD4	2001/0021970 A1	09/2001	Hotta <i>et al.</i>			05/14/2001
	AE4	2004/0054872 A1	03/2004	Nguyen <i>et al.</i>			09/12/2003
	AF4						
	AG4						
	AH4						
	AI4						
	AJ4						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK4						Yes No
	AL4						Yes No
	AM4						Yes No

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